High Speed CMOS Bus Interface 18-Bit Universal Register in QVSOP™

QS74FCT2X823T

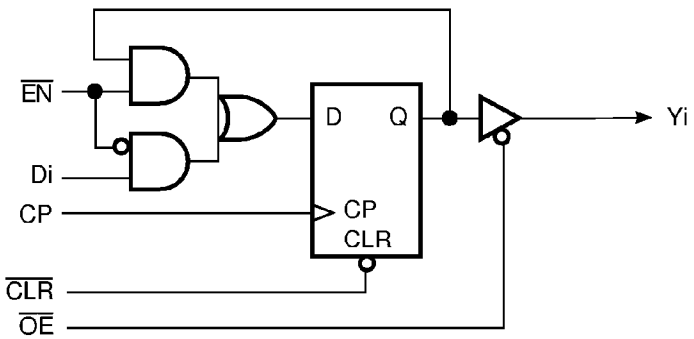
FEATURES/BENEFITS

- Function compatible to the 74F823 74FCT823 and 74FCT823T
- CMOS power levels: <15 mW static
- Undershoot clamp diodes on all inputs
- Fastest CMOS logic family available
- JEDEC-FCT spec compatible
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Available in 48-pin 0.4 mm pitch QVSOP (Q1)
- A speed grades with 10.0 ns
- I_{OL} = 48 mA Com.

DESCRIPTION

The QS74FCT2X823T is an 18-bit high-speed CMOS TTL-compatible buffered register with three-state outputs that is ideal for driving high capacitance loads such as memory and address buses. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

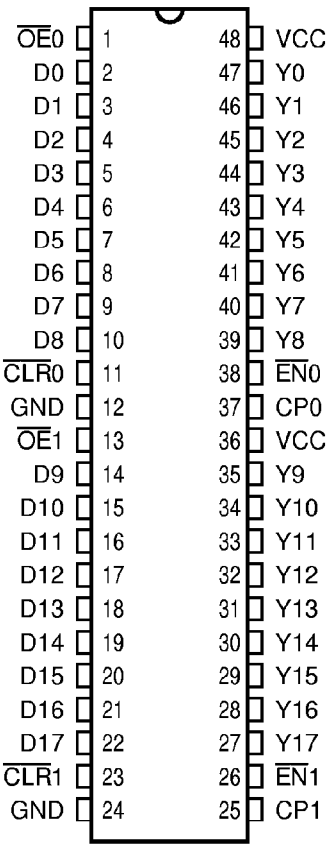


PIN DESCRIPTION

Name	I/O	Description
Di	I	Data Inputs
Yi	O	Data Outputs-Three State
CPi	I	Clock Pulse
$\overline{OE}$	I	Output Enable
$\overline{EN}$i	I	Clock Enable
$\overline{CLR}$i	I	Asynchronous Reset

PIN CONFIGURATIONS (All Pins Top View)

QVSOP



FUNCTION TABLE

Inputs					Int.	O/P	
$\overline{OE}$i	$\overline{CLR}$i	$\overline{EN}$i	Di	CPi	Qi	Yi	Function
H	X	L	L	↑	L	Hi-Z	High Z
H	X	L	H	↑	H	Hi-Z	High Z
H	L	X	X	X	L	Hi-Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Hi-Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	L	↑	L	Hi-Z	Load
H	H	L	H	↑	H	Hi-Z	Load
L	H	L	L	↑	L	L	Load
L	H	L	H	↑	H	H	Load